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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,508	02/23/2004	Christophe Chevallier	400.069US09	1475

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EXAMINER	
NGUYEN, VIET Q	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,508	CHEVALLIER, CHRISTOPHE	
	Examiner	Art Unit	
	Viet Q. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Application filed on 2/23/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,14 and 15* is/are rejected.

7)☒ Claim(s) *7-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/23/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-15** are present for examination.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1-6, and 14-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Lee et al (5,748,545) and Nagatomo (JP.411073799A).**

Lee et al (see Fig. 2) clearly shows a flash memory array (10), see col.7, and a circuit structure for testing/locating the short patterns in both the global bit lines and local bit lines. For example, Fig. 2 shows that the global bit line detector (46) is used to detect all possible shorts in the global bit lines, and the global word line short detector (41) is used to detect all possible shorts in the global word lines. With such shown structure, this reference also suggest a similar method steps for testing all adjacent, local bit lines by programming the alternate memory columns with alternating bit line stress voltages. That is, an even column or even bit line is applied first with a first logic/voltage value, and the other (or adjacent) odd column or odd bit line is applied next with an opposite logic/voltage value. One skilled in the art can see that this second opposite logic/value is obviously an inverse logic/value of the first one. The detector circuit (46, 41) will then comparing the logic pattern and generate the error signal (see

Fig. 3, GWLSOUT) indicating/locating any of such short condition presence. Note that even though Fig. 2 only labels the global bit lines as being tested, it is also shown to one skilled in the art that each such global bit line is also shown running through a specific memory column, thus each such global bit line also act/represent each local bit line, from BLIII to BLI10241, for a total of 1024 columns in such whole memory array/block (10). Thus, it would also be obvious that each memory local bit line is also being tested along with global bit lines for any column/line shorts as well.

Regarding claims **2-5**, col.9 (lines 22-35) mentions that the test pattern using high logic state for the odd bit lines and the low logic state for the even bit lines, thus obviously suggest the claimed "alternating logic high and low states" and that d' the second logic state is inverse of the first logic state" as recited.

Regarding claim **4**, col. 15 (lines 1-5) and col. 16 (lines 53-56) suggest that such testing pattern can be done in parallel, or serial, or opposite manner for all the bit lines in order if desired.

Claims **14-15** recites contain similar claimed elements of claims 1-2, and therefore are rejected for similar reasons stated above.

3. Similarly, **Nagatomo (see Fig. 3 and its constitution/description)** teaches a circuit for testing the bit line shorts in a memory array (1 10). The special memory section (120) contains the testing cells for selectively programming the even and odd columns/lines with opposite logic/voltage value. For example, the constitution stated

that ***"...by the input a testing signal WSBT, the odd number bit lines become conducting to be brought to a low level and even number bit lines reach a high level. When any line short condition exists between neighboring bit lines, these bit lines are brought to a low level"***. Thus, it would have been obvious to one skilled in this art that the special/testing memory array (12) is actually used to hold a test ***pattern*** or programming logic/values (or so-called pattern of logic states as claimed) for selectively programming and/or monitoring all the odd/even bit lines of the below memory array 110 (that needs to be tested and monitored). Furthermore, the alternating patterns of low/high logic values are also similarly used for even/odd columns, respectively, if desired, as already discussed above for the Lee patent above. Lastly, using a same testing/monitoring program/device, all such columns or bit lines could be simultaneously tested and/or monitored since each and every column/bit could be programmed individually at the same time without any undue experimentation or hardship involved.

4. Claims **7-13** contain allowable subject matter over prior arts of record in view of the specific steps of "selectively coupling odd local bit lines to odd global bit lines" and "selectively coupling even local bit lines to even global bit lines", which are not fairly suggested elsewhere or disclosed in these above references.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Viet Q Nguyen
Primary Examiner
Art Unit 2827

V. Nguyen
4/25/2005